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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,013	01/29/2004	Hiroki Shinkawata	248267US2	3634

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,013	SHINKAWATA, HIROKI	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *9-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 1-8 in the reply filed on 28 July 2005 is acknowledged. The traversal is on the ground(s) that a larger search could even be made of a large number of, or theoretically all, subclasses without substantial additional effort. This is not found persuasive because, regardless of the search, the inventions are distinct according to 35 U.S.C. 121, as described in the restriction requirement of 6 June 2005.

The requirement is still deemed proper and is therefore made FINAL.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: HIGH SPEED MEMORY DEVICE WITH REDUCED RESISTANCE AND LEAKAGE CURRENT.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. in view of JP 2003-142608. As to claim 1, Inoue et al., Figures 1-7, discloses a semiconductor substrate having a memory formation region in which a memory device is formed and a logic formation region in which a logic device is formed; a first impurity region (5) formed in an upper surface of said semiconductor substrate in said memory formation region, a second impurity region (4) formed in the

upper surface of said semiconductor substrate in said logic formation region, a third impurity region (7c) formed in an upper surface of said first impurity region and having a conductivity type different from that of said first impurity region; a fourth impurity region (7b) formed in an upper surface of said second impurity region and having a conductivity type different from that of said second impurity region; a first silicide film (12) formed in an upper surface of said third impurity region; a capacitor (15) formed above said first silicide film and electrically connected to said first silicide film; and a second silicide film (12) formed in an upper surface of said fourth impurity region. Inoue et al. does not disclose expressly that the second silicide film has a larger thickness than the first silicide film. JP 2003-142608, Figure 1, discloses (Abstract) a memory embedded DRAM semiconductor device comprising: a memory region having a memory transistor and a logic region having a logic transistor each provided in a common semiconductor substrate (1), wherein the logic transistor comprises: a gate electrode formed on the semiconductor substrate; and source/drain diffusion layers (4a) each formed in the semiconductor substrate and having a silicide film formed thereon and the memory transistor comprises a gate electrode formed on the semiconductor substrate; and source/drain diffusion layers (4b) each formed in the semiconductor substrate and having a silicide film formed thereon to be thinner than the silicide film formed on each of the source/drain diffusion layers of the logic transistor. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the logic silicide layer thicker than the memory silicide layer. The motivation for doing so would have been to reduce the wiring resistance of the logic circuit portion without increasing the leakage current in the memory cell portion, thereby reducing the power consumption of the memory (Advantage). Therefore, it would have been obvious to combine JP 2003-142608 with Inoue et al. to obtain the invention as specified in claim 1.

As to claim 2, JP 2003-142608, Figure 1, discloses first and second gate structures (2) formed on the upper surface of said semiconductor substrate in said memory formation region and spaced apart at a given distance from each other. JP 2003-142608 discloses a single gate in the logic formation region, but it is understood that there would be additional adjacent gates, which would be embodied as third and fourth gate structures, as in Inoue et al., Figure 2. Said first and second silicide films (4a) and (4b) would be provided between said first and second gate structures and between said third and fourth gate

structures, respectively. JP 2003-142608, Figure 6, discloses that a first gate aspect ratio that is defined by the distance between said first and second gate structures and a height of said first and second gate structures is larger than a second gate aspect ratio that is defined by the distance between said third and fourth gate structures and a height of said third and fourth gate structures.

Allowable Subject Matter

Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed device with a specific first gate aspect ratio.

Claims 4-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses thin third silicide regions, formed adjacent to thick second silicide regions within the logic formation region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
September 14, 2005

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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